# CMOS - INVERTER.

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It consists of p-MOS and N-MOS FET. The input A serve as the gate voltage for both transistors. The inverter circuit is shown below.

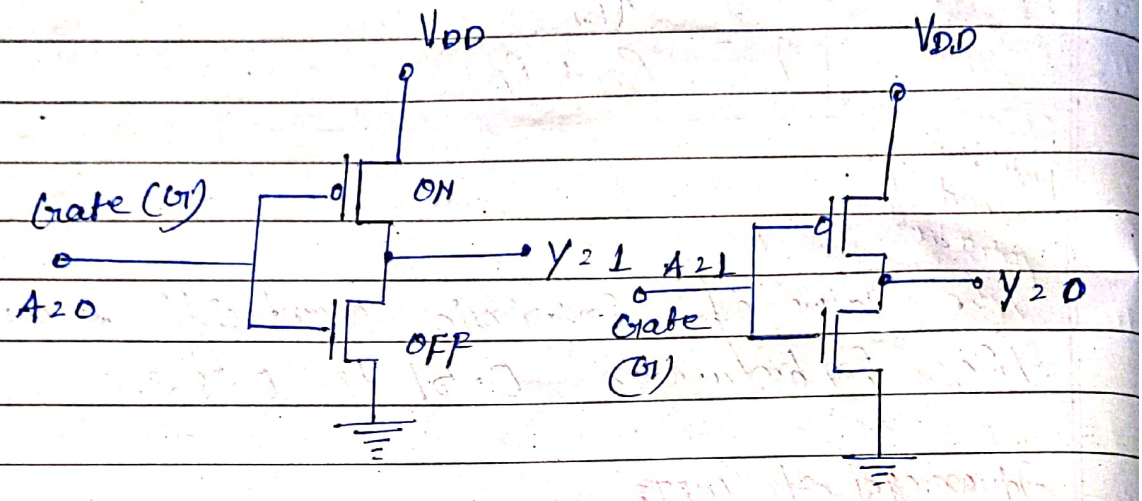


Fig: CMOS - INVERTER.

The NMOS transistor has an input from Vss (ground) and PMOS transistor has an input from VDD. The terminal Y is output terminal.

**Operation:**

I) When a high voltage (VDD) is given at the input terminal (A) of the inverter, the PMOS becomes open and N-MOS becomes closed so, the output will be ~~low~~ zero. (logic 0).

II) When a low voltage (0V) is applied to the gate of the inverter, the NMOS is turned OFF and P-MOS turned ON. So the output of the inverter is pulled to VDD i.e logic 1.

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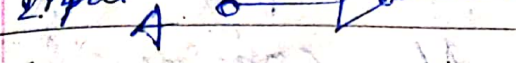


| Input A | output y |
|---|---|
| 0 | 1 |
| 1 | 0 |